CLAIMS

1. A memory circuit comprising:

one or more magnetoresistive random access memories, MRAMs, coupled to a flip-flop circuit.

2. A memory circuit according to claim 1, comprising two MRAMs and the flip-flop circuit, the flip-flop circuit comprising two inputs, each of the two MRAMs being coupled to a respective one of the flip-flop circuit inputs.

3. A display device comprising a plurality of pixels and a plurality of memory circuits according to claim 1 or 2, each pixel being associated with a respective one of the memory circuits.

4. A pixel and memory assembly for a display device, comprising:

a pixel display electrode coupled to in-pixel memory means, the in-pixel memory means comprising one or more MRAMs.

5. The pixel and memory assembly according to claim 4, wherein the in-pixel memory means further comprises a flip-flop circuit, the one or more MRAMs being coupled to the flip-flop circuit.

6. The pixel and memory assembly according to claim 5, comprising two MRAMs and the flip-flop circuit, the flip-flop circuit comprising two inputs, each of the two MRAMs being coupled to a respective one of the flip-flop circuit inputs.

7. A pixel and in-pixel memory for a display device, comprising:

a switching device;

a pixel electrode;

a first MRAM;

a second MRAM; and

a bit line, the bit line running from the switching device to the pixel electrode;

the bit line being arranged to cross over the first MRAM in a first direction and to cross over the second MRAM in a second direction, the first direction being substantially opposed to the second direction.

8. A pixel and in-pixel memory for a display device according to claim 7, wherein the bit line passes over the first MRAM then turns or meanders back on itself before passing over the second MRAM.

9. A pixel and in-pixel memory for a display device according to claim 7 or 8, wherein the bit line connects with a respective one end of each of the first and second MRAMs; and further comprising:

a word line, running under the other ends of each of the first and second MRAMs, for addressing the MRAMs; and

a gate line, for driving the switching device, coupled to the switching device;

the word line being arranged between the pixel electrode and the gate line such that the bit line passes over the word line but does not pass over the gate line.

10. A pixel and in-pixel memory for a display device, comprising:

a switching device;

a pixel electrode;

one or more MRAMs;

a bit line running from the switching device to the pixel electrode via one end of each of the one or more MRAMs;

a word line, running under the other ends of each of the one or more MRAMs, for addressing the MRAMs; and

a gate line, for driving the switching device, coupled to the switching device;

the word line being arranged between the pixel electrode and the gate line such that the bit line passes over the word line but does not pass over the gate line.

11. A display device comprising a pixel and in-pixel memory according to any of claims 7 to 10.

12. A display device according to claim 11, wherein the pixel and in-pixel memory is integrated with active matrix elements and drive lines of the display device.

13. A method of forming an in-pixel memory display device, comprising:

forming a switching device;

forming an in-pixel memory circuit comprising one or more MRAMs coupled to a read-out circuit;

forming a word line, for addressing the in-pixel memory circuit; and

forming a gate line, for driving the switching device;

wherein the word line and the gate line are formed during a same masking stage.

14. A method of forming an in-pixel memory display device, comprising:

forming a switching device;

forming an in-pixel memory circuit comprising one or more MRAMs coupled to a read-out circuit;

forming a bit line, for addressing the in-pixel memory circuit; and

forming a column line, for driving the switching device;

wherein the bit line and the column line are formed during a same masking stage.

15. A method of forming an in-pixel memory display device, according to claim 14, further comprising:

forming a word line, for addressing the in-pixel memory circuit; and

forming a gate line, for driving the switching device;

wherein the word line and the gate line are formed during a further same masking stage.

16. A method of forming an in-pixel memory display device, according to any of claims 13 to 15, wherein the in-pixel memory circuit further comprises a flip-flop circuit.